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EXAMINER	
TANG, KUO LIANG J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,459	HINES, KENNETH J.	
	Examiner	Art Unit	
	Kuo-Liang J Tang	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19, 26-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/25/04, 9/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 10/08/04*.

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 10/7/2004.

The priority date of this application is 6/23/2000.

Claims 1-18 and 20-25 are cancelled. Claims 26-43 are added. Claim 19 is amended.

Claims 19 and 26-43 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 8/25/2004 and 10/08/2004 are being considered by the examiner.

The information disclosure statement (IDS) submitted on 9/15/2004, only US-6,038,381 and US-6,134,676 are being considered by the examiner. The rest of the documents are duplicated and filed on 8/25/2004.

Specification

3. The examiner has no idea what to handle the "cross reference to the related applications" submitted on 10/11/2004 and 10/18/2004. The Applicant is required to specifies more instructions on where and / or how to insert these two tables into the specification.

Response to Arguments

4. Applicant's arguments with respect to claims 19 and 26-43 have been considered but are moot in view of the new ground(s) of rejection.

Claims 19, 35-40 and 43 are rejected under 35 U.S.C. §101.

Claims 19, 26-39, 41-43 are rejected under 35 U.S.C. 102(a) as being anticipated by Munch et al. US Patent No. 6,038,381 (hereinafter Munch).

Claim 40 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Argument, the applicant indicates that:

I) The Office Action rejects claims 1-7 and 19-25 under U.S.C. § 101 as being directed to nonstatutory subject matter. The claim amendments in this response overcome this rejection. (See ARGUMENT, page 16, lines 10-13).

II) As per Claim 26, Munch does not recite a data structure and the directed edges represent potential influences of input nodes on output nodes, and claim 26 recites various specific behaviors for directed edges (See ARGUMENT, page 17, 1st paragraph).

III) As per Claim 19, Munch does not teach "creating, for each new conjunctive node that generates and output value, a new outgoing edge from the new conjunctive node to a corresponding disjunctive node" (See ARGUMENT, page 17, 2nd paragraph).

Examiner's response:

I) The examiner does not agree Applicant's amendment overcomes 101 rejection. In fact, Claim 19 only changes from "comprising the steps of" to "comprising", which still not overcome the 101 rejection.

II) Munch discloses "a data structure encoded in the machine accessible medium, the data structure comprising:

'conjunctive nodes (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard) and disjunctive nodes " (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)) that represent characteristics of a software system (E.g. see col. 1:16-18, EDA system)'; and

'directed edges connecting the conjunctive nodes and the disjunctive nodes, wherein: each of the directed edges connects two nodes as an input node to said directed edge and an output node to said directed edge (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges))';

'each directed edge represents a potential influence of the input node on the output node' (E.g. see FIG. 6 and associated text); and

'the directed edges comprise two or more edges selected from the group consisting of:

an edge that is enabled by a true value from the input mode and, when enabled, produces a true value for the output node' (E.g. see FIG. 7B, AND gate 422, input A, output C and associated text);

'an edge that is enabled by a true value (E.g. see FIG. 6, gate 352, SEL2 264 and associated text) from the input mode and, when enabled, produces a false value for the output node (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text);

an edge that is enabled by a false value from the input mode (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text) and, when enabled, produces a true value for the output node (E.g. see FIG. 6, AND gate 356 output to OR gate 358 and associated text); and

an edge that is enabled by a false value from the input mode and, when enabled, produces a false value for the output node'' (E.g. see FIG. 7C, OR gate 426 and associated text, if both inputs A and B are FALSE value, then the output C is FALSE value too).

III) Munch discloses "creating, for each new conjunctive node that generates and output value, a new outgoing edge from the new conjunctive node to a corresponding disjunctive node" (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges) and FIG. 6, output of AND (conjunctive node) gate 354 to OR gate 358 (disjunctive node) and associated text).

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 19, 35-40 and 43 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As Per Claim 19, claim is non-statutory because it is program listing per se / non-functional descriptive material. Not in the useful or technological arts and therefore not patent eligible subject matter.

As Per Claim 35, claim is non-statutory because it is non-functional descriptive material. Not in the useful or technological arts and therefore not patent eligible subject matter.

Claim 43, which depend from claim 19 is also rejected under 35 U.S.C. 101 for the same reason.

Claims 36-40, which depend from claim 35 are also rejected under 35 U.S.C. 101 for the same reason.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C 101 (nonstatutory) above are further rejected as set forth below in application of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 19, 26-39, 41-43 are rejected under 35 U.S.C. 102(a) as being anticipated by Munch et al. US Patent No. 6,038,381 (hereinafter Munch).

As Per Claim 19, Munch discloses a Method and system for determining a signal that controls the application of operands to a circuit-implemented function for power savings. (See Abstract & FIG 8, 9 and associated text). In that Munch discloses the method of creating data structure that covering the steps of:

"creating a new disjunctive node (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)) for each node in the software system (E.g. see col. 1:16-18, EDA system)";

"creating a new conjunctive node for each pair if corresponding constraints in the software system" (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard);

"creating, for each new conjunctive node that generates and output value, a new outgoing edge from the new conjunctive node to a corresponding disjunctive node" (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges) and FIG. 6, output of AND (conjunctive node) gate 354 to OR gate 358 (disjunctive node) and associated text); and

"creating, for each new disjunctive node that generates an output value, a new outgoing edge from the new disjunctive node to a corresponding conjunctive node" (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges)).

As Per Claim 26, Munch discloses a Method and system for determining a signal that controls the application of operands to a circuit-implemented function for power savings. (See Abstract & FIG 8, 9 and associated text). In that Munch discloses the method of creating data structure that covering the steps of:

"a machine accessible medium" (E.g. see FIG. 2, Data Storage Device 104 and associated text); and

"a data structure encoded in the machine accessible medium, the data structure comprising:

'conjunctive nodes (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard) and disjunctive nodes " (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)) that represent characteristics of a software system (E.g. see col. 1:16-18, EDA system)'; and

'directed edges connecting the conjunctive nodes and the disjunctive nodes, wherein: each of the directed edges connects two nodes as an input node to said directed edge and an output node to said directed edge (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges))';

'each directed edge represents a potential influence of the input node on the output node' (E.g. see FIG. 6 and associated text); and

'the directed edges comprise two or more edges selected from the group consisting of:

an edge that is enabled by a true value from the input mode and, when enabled, produces a true value for the output node' (E.g. see FIG. 7B, AND gate 422, input A, output C and associated text);

'an edge that is enabled by a true value (E.g. see FIG. 6, gate 352, SEL2 264 and associated text) from the input mode and, when enabled, produces a false value for the output node (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text);

an edge that is enabled by a false value from the input mode (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text) and, when enabled, produces a true value for the output node (E.g. see FIG. 6, AND gate 356 output to OR gate 358 and associated text); and

an edge that is enabled by a false value from the input mode and, when enabled, produces a false value for the output node'' (E.g. see FIG. 7C, OR gate 426 and associated text, if both inputs A and B are FALSE value, then the output C is FALSE value too).

As per Claim 27, the rejection of claim 26 is incorporated and further Munch teaches: "wherein each of the disjunctive nodes represents a Boolean guard on a functional object within the software system" (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)).

As per Claim 28, the rejection of claim 26 is incorporated and further Munch teaches:

"wherein each of the conjunctive nodes represents a Boolean guard on a state change within the software system" (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard).

As per Claim 29, the rejection of claim 26 is incorporated and further Munch teaches:

"wherein each of the disjunctive nodes represents a node in the software system" (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)).

As per Claim 30, the rejection of claim 26 is incorporated and further Munch teaches:

"wherein each of the conjunctive nodes represents a pair of constraints in the software system" (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard and see FIG. 8A step 545 and associated text).

As Per Claim 31, Munch discloses a Method and system for determining a signal that controls the application of operands to a circuit-implemented function for power savings. (See Abstract & FIG 8, 9 and associated text). In that Munch discloses the method of creating data structure that covering the steps of:

"a machine accessible medium" (E.g. see FIG. 2, Data Storage Device 104 and associated text); and

"a software analysis tool (E.g. see col. 18:50-57) encoded in the machine accessible medium, the software analysis tool comprising instructions to produce, as output, a graph that exposes control interactions between software elements of a software system, the graph comprising: conjunctive nodes (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..." (conjunctive boolean guard)) and disjunctive nodes (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..." (disjunctive boolean guard)) that represent characteristics of a software system (E.g. see col. 1:16-18, EDA system) that represent characteristics of the software system"; and

"directed edges connecting the conjunctive nodes and the disjunctive nodes, wherein: each of the directed edges connects two nodes as an input node to said directed edge and an output node to said directed edge; each directed edge represents a potential influence of the input node on the output node" (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ..." (directed edges)); and

"the directed edges comprise two or more edges selected from the group consisting of:

an edge that is enabled by a true value from the input mode and, when enabled, produces a true value for the output node (E.g. see FIG. 7B, AND gate 422, input A, output C and associated text);

an edge that is enabled by a true value (E.g. see FIG. 6, gate 352, SEL2 264 and associated text) from the input mode and, when enabled, produces a false value for the output node (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text);

an edge that is enabled by a false value from the input mode (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text) and, when enabled, produces a true value for the output node (E.g. see FIG. 6, AND gate 356 output to OR gate 358 and associated text); and

an edge that is enabled by a false value from the input mode and, when enabled, produces a false value for the output node'' (E.g. see FIG. 7C, OR gate 426 and associated text, if both inputs A and B are FALSE value, then the output C is FALSE value too).

As per Claims 32-33, the rejection of claim 31 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 28 and 27 respectfully.

As per Claim 34, the rejection of claim 31 is incorporated and further Munch teaches:

"wherein the directed edges represent implication between the conjunctive nodes and the disjunctive nodes" (E.g. see FIG. 6, AND gate 354 and OR gate 358 and associated text).

As Per Claim 35, Munch discloses a Method and system for determining a signal that controls the application of operands to a circuit-implemented function for power savings. (See Abstract & FIG 8, 9 and associated text). In that Munch discloses the method of creating data structure that covering the steps of a method comprising:

"generating conjunctive nodes and disjunctive nodes to represent characteristics of a software system" (E.g. see FIG. 6 and associated text); and

"generating directed edges to connect the conjunctive nodes (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ...") and the disjunctive nodes (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ..."), wherein:

each of the directed edges connects two nodes as an input node to said directed edge and an output node to said directed edge (E.g., see col. 7:58-67 & 8:1-5 which states "...interconnected with signal lines (e.g., 234, 252, 272). ...");

each directed edge represents a potential influence of the input node on the output node (E.g. see FIG. 6 and associated text); and

the directed edges comprise two or more edges selected from the group consisting of:

an edge that is enabled by a true value from the input mode and, when enabled, produces a true value for the output node (E.g. see FIG. 7B, AND gate 422, input A, output C and associated text);

an edge that is enabled by a true value (E.g. see FIG. 6, gate 352, SEL2 264 and associated text) from the input mode and, when enabled, produces a false value for the output node (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text);

an edge that is enabled by a false value from the input mode (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text) and, when enabled, produces a true value for the output node (E.g. see FIG. 6, AND gate 356 output to OR gate 358 and associated text); and

an edge that is enabled by a false value from the input mode and, when enabled, produces a false value for the output node'' (E.g. see FIG. 7C, OR gate 426 and

associated text, if both inputs A and B are FALSE value, then the output C is FALSE value too).

As per Claim 36, the rejection of claim 35 is incorporated and further Munch teaches:

"generating, as output, a graph that includes at least one of the conjunctive nodes, at least one of the disjunctive nodes, and at least one of the directed edges" (E.g. see FIG. 6 and associated text).

As per Claim 37, the rejection of claim 35 is incorporated and further Munch teaches:

"debugging debug the software system, based at least in part on analysis of the conjunctive nodes, disjunctive nodes, and directed edges" (E.g. see col. 2:61-63).

As per Claim 38, the rejection of claim 35 is incorporated and further Munch teaches:

"wherein the operations of generating conjunctive nodes, disjunctive nodes, and directed edges are performed in a data processing system, the method further comprising: identifying a constraint conflict within the software system, based at least in part on the conjunctive nodes, disjunctive nodes, and directed edges generated in the data processing system" (E.g. see col. 9:40-58).

As per Claim 39, the rejection of claim 35 is incorporated and further Munch teaches:

"storing the conjunctive nodes, disjunctive nodes, and directed edges in a data processing system" (E.g. see FIG. 2, Data Storage Device 104 and associated text).

As Per Claim 41, Munch discloses a Method and system for determining a signal that controls the application of operands to a circuit-implemented function for power savings. (See Abstract & FIG 8, 9 and associated text). In that Munch discloses the method of creating data structure that covering the steps of an apparatus comprising:

"a machine accessible medium" (E.g. see FIG. 2, Data Storage Device 104 and associated text); and

"instructions encoded in the machine accessible medium to implement a software tool that supports detection of constraint enforcement conflicts in a software system, the software tool performing operations comprising:

creating a disjunctive node for at least one mode in the software system (E.g., see col. 13:4-14 which states "... disjunctive Boolean expression (e.g., OR) is used. ...");

creating a conjunctive node for at least one pair of corresponding constraints in the software system (E.g., see col. 13:9-26 which states "...the conjunctive Boolean expression, AND, is used because node 588 has only one fan-out. ..."); and

creating, for each conjunctive node that generates an output value, an outgoing edge from the conjunctive node to a corresponding disjunctive node (E.g. see FIG. 6 and associated text).

As per Claim 42, the rejection of claim 41 is incorporated and is rejected under the same reason set forth in connection of the rejection of claim 38.

As per Claim 43, the rejection of claim 19 is incorporated and further Munch teaches:

"each of the directed edges connects two nodes as an input node to said directed edge and an output node to said directed edge" (E.g. see FIG. 6 and associated text);

"each directed edge represents a potential influence of the input node on the output node" (E.g. see FIG. 6 and associated text); and

"the directed edges comprise two or more edges selected from the group consisting of:

an edge that is enabled by a true value from the input mode and, when enabled, produces a true value for the output node (E.g. see FIG. 7B, AND gate 422, input A, output C and associated text);

an edge that is enabled by a true value (E.g. see FIG. 6, gate 352, SEL2 264 and associated text) from the input mode and, when enabled, produces a false value for the output node (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text);

an edge that is enabled by a false value from the input mode (E.g. see FIG. 6, gate 352 output to AND gate 356 and associated text) and, when enabled, produces a true value for the output node (E.g. see FIG. 6, AND gate 356 output to OR gate 358 and associated text); and

an edge that is enabled by a false value from the input mode and, when enabled, produces a false value for the output node'' (E.g. see FIG. 7C, OR gate 426 and associated text, if both inputs A and B are FALSE value, then the output C is FALSE value too).

Allowable Subject Matter

9. Claim 40 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuo-Liang J Tang whose telephone number is (571) 272-3705. The examiner can normally be reached on 8:30AM - 7:00PM (Monday – Thursday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kuo-Liang J. Tang

Software Engineer Patent Examiner

TUAN DAM
SUPERVISORY PATENT EXAMINER